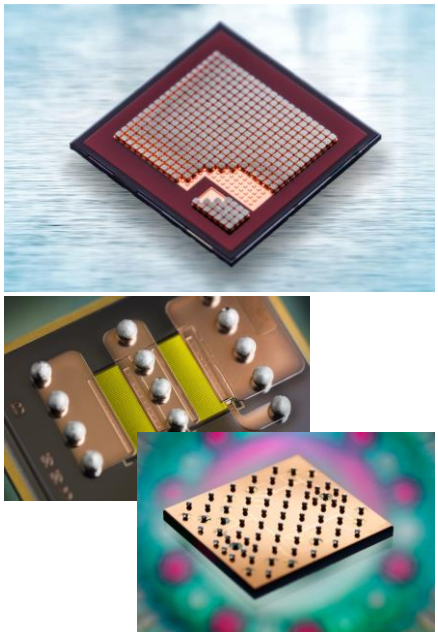
Fraunhofer
IZM

FRAUNHOFER INSTITUTE FOR RELIABILITY AND MICROINTEGRATION IZM



Thin SiC JFET (100 µm) with 80 µm thick electroplated copper (top), GaN based half-bridge fabricated by wafer level silicon embedding (middle), RF System-in-Package with embedded GaN HPA, Driver, their silicon decoupling capacitors and thermal sensor (bottom)

Fraunhofer Institute for Reliability and Microintegration IZM
Gustav-Meyer-Allee 25,
13355 Berlin,
Germany

Contact
Hermann Oppermann
Phone +49 30 46403-163
oppermann@izm.fraunhofer.de

Charles-Alix Manier
Phone +49 30 46403-612
charles-alix.manier@izm.fraunhofer.de

www.izm.fraunhofer.de

Wafer Level Packaging of Power Devices

Emerging applications, growing market segments and upcoming breakthrough of wide-band gap semiconductor technologies like e.g. SiC or GaN for better cost and global energetic efficiencies (i.e. from device fabrication to field application), are inevitably leading to higher requirements in terms of current densities, thermal management and packaging technologies. In order to address increasing power density of bare semiconductors and simultaneously higher module compactness, novel concepts, including new materials and joining technologies must be developed for extracting the highest potential of WBG semiconductors or next generations of Si Power semiconductors.

Tackling aggressive operating conditions requires wafer level packaging and interconnect technologies that deliver both electrical pathways with high current-carrying capacity and temperature-resistant above 250 °C. New packaging topologies are necessary, beyond the well established packaging topology, which relies on direct die bonding of the bare devices and wire bonds. For this, semiconductors must be to one point further customized by post-processing (back end) so to re-shape the electrical contacts in terms of final metallisations or geometry (pad extension, thickness).

Fraunhofer IZM disposes of up to 300 mm manufacturing processes compatible with common wafer-level packaging techniques and are essentially based on conventional wafer bumping using electrodeposition. Amongst others **thick electroplated copper** has been developped up to 100 µm with excellent structure resolution, high planarity and low mechanical stress. For certain semiconductor materials, **gold** and gold/tin, or even **nanoporous gold** are used instead of copper. Minimized roughness and surface modifications extend the technology's possibilities to thermocompression and ultrasonic bonding at reduced bond force and low temperature. Apart from conventional silicon wafers, Fraunhofer IZM's thin-film technology can handle almost all types of semiconductor materials, from SiC, GaN, GaAs, Ge, InP to glass and polymer wafers.

Besides device post-processing, Fraunhofer IZM offers the developments of wafer level packaging solutions in **compact heterogenous integration**, for instance based on embedding technologies in silicon carrier wafers taking advantage for power applications of the substantial thermal conductiviy of silicon as a base material for electronic packages. Silicon can even be structured to realise cooling interposers with channels for liquid cooling at the nearest of the power source.